

## REPLACEMENT SECTION (MARKED UP COPY)

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of the monitoring system according to a preferred embodiment of the present invention.

FIG. 2-00 is another perspective view of the monitoring system according to a preferred embodiment of the present invention.

FIG. 2-01 through FIG. 2-89 provide detailed descriptions of a preferred embodiment of the present invention.

FIG. 3, comprising FIG. 3A, FIG. 3B, FIG. 3C., and FIG. 3D, is a perspective view of a Second logic-processor according to a preferred embodiment of the present invention.

FIG. 4 is a Receiver flowchart according to a preferred embodiment of the present invention.

FIG. 5, comprising FIG. 5A and FIG. 5B, is a perspective view of a power source according to a preferred embodiment of the present invention.

FIG. 6-00 is a perspective view of an electric circuit according to a preferred embodiment of the present invention.

FIG. 6-01 is another perspective view of an electric circuit according to a preferred embodiment of the present invention.

FIG. 7, comprising FIG. 7A, FIG. 7B, FIG. 7C., and FIG. 7D, is a wireless system configurations table according to a preferred embodiment of the present invention.

FIG. 8 is a firmware flowchart according to a preferred embodiment of the present invention.

FIG. 9 is a perspective view of a network coupler according to a preferred embodiment of the present invention.

FIG. 10, comprising FIG. 10A and FIG. 10B, is a sensor sampling-plan according to a preferred embodiment of the present invention.

FIG. 11 is a perspective view of a Second logic-processor according to another preferred embodiment of the present invention.

FIG. 12, comprising FIG. 12A and FIG. 12B, is an alternative perspective view of a

Second logic-processor according to a preferred embodiment of the present invention.

FIG. 13, comprising FIG. 13A and FIG. 13B, is a side view of the sections of a Second logic-processor according to a preferred embodiment of the present invention.

FIG. 14, comprising FIG. 14A and FIG. 14B, is a posterior view of the sections of a Second logic-processor for according to a preferred embodiment of the present invention.

Within the specification, reference to a figure number indicates reference to the set of all lettered figures for that number (for example, reference to “FIG. 7” indicates reference to FIG. 7A, FIG. 7B, FIG. 7C., and FIG. 7D).

## REMARKS

Reconsideration is respectfully requested.

Applicant is submitting replacement drawings for ALL figures and ALL sheets to correct formatting problems identified in the Draftperson's Patent Drawing Review. The specification has also been amended to renumber the figures to the extent necessitated by the corrections made per the Draftperson's Patent Drawing Review. No substantive changes have been made to the specification or drawings, and no new matter has been added.

Per the Draftperson's Patent Review, the following corrections have been made to the drawings:

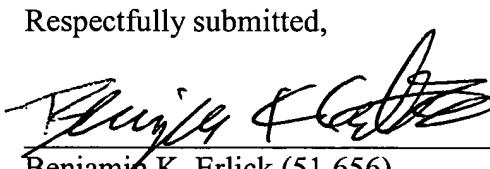
- ξ Margins have been corrected for ALL drawings
- ξ Views have been properly labeled for FIGS. 2-29, 2-31, 2-32, 2-34 through 2-39, 2-41, 2-43, 3, 5, and 12-14.
- ξ Heavy black shading has been removed
- ξ Figure legends have been placed correctly
- ξ Sheet numbers have been placed properly
- ξ Line quality/legibility has been corrected for lines, numbers, and letters for ALL drawings.
- ξ Numbers and reference characters have been corrected for quality/legibility
- ξ Additional formatting changes have been made to make corrections in response to other comments listed in the Draftperson's Patent Drawing Review.

Applicant believes that all Drawings, as corrected, now conform to USPTO requirements.

If there are any fees incurred by this Amendment Letter, please deduct them from our Deposit Account NO. 50-1887.

Respectfully submitted,

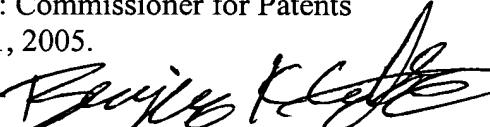
Date: July 21, 2005

  
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I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail (label EV 632758249 US) addressed to: Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 on July 21, 2005.

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Name of Registered Representative:

Signature: 

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